TITLE OF THE INVENTION

SIC SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates to a SiC semiconductor device that is metal-insulator-semiconductor (MIS) field-effect transistor fabricated on a silicon carbide substrate. It particularly relates to a SiC semiconductor device having al optimized impurity diffusion layer and a defined substrate crystal plane orientation.

DESCRIPTION OF THE PRIOR ART

[0002] Silicon carbide has an energy gap that is two to three times larger than that of silicon and a breakdown voltage that is about three times higher. Silicon carbide is being viewed as the substrate material for the next generation of transistors for high-power, high-temperature and high-frequency applications. In particular, considerable expectations are being placed on metal-insulator-semiconductor field-effect transistors (MISFETs) for use as switching devices, since MISFETs are faster than bipolar transistors.

[0003] However, when a silicon carbide substrate is used, the interface between the oxide and the silicon carbide has an interface level density that is approximately one magnitude higher than that of a silicon MIS transistor. Thus, there is the problem that an MIS field-effect transistor that uses a silicon carbide substrate has a channel mobility that is approximately one magnitude lower than an MIS field-effect transistor that has a silicon substrate.

[0004] To make silicon MIS transistors less susceptible to the effect of the interface between the oxide layer and silicon carbide when electrons are flowing from the source to the drain, an MIS field-effect transistor having a buried channel region is known to exhibit excellent characteristics. However, in the case of an MIS transistor on a silicon carbide substrate, so far the optimization of buried channel region transistors has not been adequate, and have tended to operate as normally on (a state in which there is still a current flow between source and drain even when there is zero gate voltage), making the device difficult to use. Moreover, MIS transistors that are not normalized have poor hot-carrier endurance that results in inadequate punch-through endurance.

[0005] A number of inventions have been disclosed for improving the characteristics of buried channel MIS field-effect transistors. USP 5,864,157, for example, describes a double-gate flash memory that uses a P-type lower gate and an N-impurity in a buried channel region. However, since this only relates to a double-gate flash memory, it is different from the structure of the present invention. Moreover, the disclosure does not touch either on the concentration of the P-type polycrystalline silicon electrode and the impurity concentration of the buried channel region, or on the relationship of the depth of the source and drain regions and the depth of the channel region.

[0006] JP-A Hei 8-186179 describes an N-channel transistor having a lightly doped drain (LDD) structure with a P-gate and an N-doped buried channel region. However, the disclosure does not describe either the concentration of the P-type polycrystalline silicon electrode, or the relationship between the depths of the source and drain regions and the depth of the channel region. Similarly, JP-A Hei 7-131016 describes an MIS field-effect transistor characterized in that the channel formation face is parallel to the (11-20) surface of the hexagonal silicon carbide single-crystal substrate. However, the disclosure does not describe a buried channel region MIS field-effect transistor that uses a P-type gate.

[0007] An object of the present invention is to provide a SiC semiconductor device that is a buried channel region MIS transistor that is not put into a normally on state by optimization of the buried channel region type MIS transistor structure or silicon carbide substrate crystal plane orientation, and has high hot-carrier endurance, high punch-through endurance and high channel mobility.

SUMMARY OF THE INVENTION

[0008] To attain the above object, the present invention provides a SiC semiconductor device comprising a semiconductor substrate having a P-type silicon carbide region, a gate insulation layer formed on the silicon carbide region, a P-type gate electrode formed on the gate insulation layer, an N-type impurity region having an impurity concentration sufficient to form a buried channel region in a semiconductor layer on a lower surface of the gate insulation layer, and source and drain regions comprised of N-type impurity regions formed adjacent to the gate insulation layer and gate electrode.

[0009] The invention also comprises the above device in which, in order to optimize the depth of the buried channel region and achieve high mobility, the ratio (L_{bc}/X_j) is not less

than 0.2 and not more than 1.0, where the L_{bc} is the depth from the interface between the gate insulation layer and the silicon carbide to the buried channel region, and the X_j is the depth from the interface between the gate insulation layer and the silicon carbide to the source and drain region junction.

[0010] The invention also comprises the device described above in which the gate electrode is comprised of polycrystalline silicon in which boron or aluminum is diffused at a concentration within a range 1 x 10^{16} cm^{-3} to 1 x 10^{21} cm^{-3}.

[0011] The invention also comprises the above device in which the buried channel region contains a diffusion of nitrogen, phosphorus, or arsenic at a maximum concentration that is from 5 x 10^{15} cm^{-3} to 1 x 10^{18} cm^{-3}.

[0012] The invention also comprises the above device in which the gate includes a silicide layer of a refractory metal.

[0013] The invention also comprises the above device in which the refractory metal is tungsten, molybdenum or titanium.

[0014] The invention also comprises the above device in which, between the buried channel region and the source and drain regions, there is a region having an impurity concentration that is not lower than a maximum impurity concentration of the impurity layer region used to form the buried channel region and not higher than an impurity concentration of the source or drain regions.

[0015] The invention also comprises the above device in which there is included, between the buried channel region and the source and drain regions, a diffusion layer of nitrogen, phosphorus or arsenic at a maximum concentration that is from 5 x 10^{16} cm^{-3} to 5x 10^{19} cm^{-3}.

[0016] The invention also comprises the above device in which, located adjacently under the buried channel formation region is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate.

[0017] The invention also comprises the above device that has a high-concentration P-type impurity diffusion region located adjacently under the buried channel region that includes an aluminum or boron diffusion layer having a maximum impurity concentration of 1 x 10^{17} cm^{-3} to 1 x 10^{19} cm^{-3}.

[0018] The invention also comprises the above device that is formed on a (11-20) surface of a hexagonal or rhombohedral or a (110) surface of a cubic system silicon carbide crystal in order to improve the channel mobility.

[0019] The invention also comprises the above device that has a lateral resurf or lateral DMOS type MOSFET structure.

[0020] The invention also comprises the above device that has a DMOS type MOSFET structure.

[0021] The invention also comprises the above device in which the gate electrode is formed of aluminum or an alloy that contains aluminum.

[0022] Further features of the invention, its nature and various advantages will be more apparent from the following detailed description which is to be read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Figure 1 depicts the steps of fabricating a MIS field-effect transistor having a P-type gate electrode and buried channel region.

[0024] Figure 2 is a measured result showing the relationship between channel mobility and threshold voltage in a MIS field-effect transistor with a gate electrode of P-type polycrystalline silicon, N-type polycrystalline silicon, and aluminum.

[0025] Figure 3 is a measured result showing the L_{bc}/X_j dependency of the channel mobility of the buried channel, with a P-type polycrystalline silicon gate electrode.

[0026] Figure 4 is a measured result showing the relationship between the impurity concentration of the polycrystalline silicon gate and the threshold voltage.

[0027] Figure 5 is a measured result showing the relationship between channel mobility and the impurity concentration of the buried channel region.

[0028] Figure 6 is a sectional view of a lateral resurf or lateral DMOS type MOSFET.

[0029] Figure 7 is a sectional view of a lateral resurf or lateral DMOS type MOSFET with a well.

[0030] Figure 8 is a sectional view of a DMOS type MOSFET.

[0031] Figure 9 is a sectional view of another DMOS type MOSFET.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0032] This invention is intended mainly for high-power transistors. There are various high-power transistors that use silicon substrates, and it is known that similar properties can be achieved using SiC substrates. The MOSFET shown in Figure 6, which is referred to as a lateral resurf or lateral DMOS type MOSFET, is one such transistor. In the following, the structure and fabrication of this transistor are described.

Example 1:

[0033] Figure 1(a) shows a P-type silicon carbide substrate 1 (4H-SiC, impurity concentration: 5×10^{15} cm^{-3}). After the substrate 1 was subjected to RCA cleaning, reactive ion etching (RIE) was used to form photolithography alignment marks on the substrate. Next, in order to investigate the punch-through endurance improvement effect, aluminum ion implantation was used to form a punch-through prevention region 3 at a depth that placed the region below the buried channel region. At 1×10^{16} cm^{-3} to 1×10^{19} cm^{-3}, the punch-through prevention region was given a higher aluminum concentration than that of the substrate 1. A number of samples were thus prepared.

[0034] The next step was to form the buried channel region 2, which was done using ion implantation of an N-type impurity such as nitrogen, phosphorus or arsenic. To use phosphorus to form a buried channel region at a junction depth (L_{bc}) of 0.3 μm, for example, the desired profile is formed using multiple implantations at 40 keV to 250 keV to provide a total dose to achieve a concentration of 7×10^{15} cm^{-3}. To investigate the relationship between the channel mobility and the ratio between the depth (X_j) of the source 5 or drain 6 (Figure 1(b)) and L_{bc}, buried channel regions 2 were formed at depths (L_{bc}) of 0.1, 0.2, 0.3, 0.4 and 0.5 μm. To investigate the concentration dependency of the buried channel region 2 with respect to channel mobility, ion implantation was used to prepare samples having concentrations ranging from 5×10^{15} cm^{-3} to 5×10^{17} cm^{-3} at an L_{bc} of 0.3 μm.

[0035] Subsequently, to form an ion implantation mask 4 for the source and drain regions shown in Figure 1(b), thermal oxidation or chemical vapor deposition (CVD) was used to form a SiO_2 layer. As shown in Figure 1(b), a low-temperature oxide (LTO) layer was used for the implantation mask. The LTO layer was formed by reacting silane and oxygen at 400°C to 800°Cto form silicon dioxide, which was deposited on the substrate 1. Then, after using photolithography to form the source and drain regions, hydrofluoric acid

was used to etch the LTO and open the source/drain regions. Next, to form the source 5 and drain 6, ion implantation at 500°C was used to implant nitrogen, phosphorus or arsenic at a depth (X_j) of 0.5 μm. In this example, as in the case of the buried channel region 2, multiple implantation steps were used to form a phosphorus concentration of 5×10^{19} cm^{-3}. This was followed by activation annealing for 30 minutes at 1500°C in an argon atmosphere. This was followed by oxidation at 1200°C for 150 minutes, forming a gate insulation layer 7 approximately 50 nm thick. After annealing for 30 minutes in an argon atmosphere, the samples were cooled in argon to room temperature.

[0036] Next came the forming of P-type gate electrode 8. Described below are a number of methods for this.

1) P-type polycrystalline silicon can be formed using the CVD method to form polycrystalline silicon, and then using boron or boron fluoride ion implantation.

2) The P-type polycrystalline silicon can be formed by using the CVD method to form polycrystalline silicon, followed by the formation of a boron-containing SiO_2 film by the CVD method or by spin-coating, and using heat-treatment at 800°C to 1100°C to effect diffusion.

3) The P-type polycrystalline silicon is formed by running silane and diborane together and heating them at 600°C, to grow the polycrystalline silicon while diffusing boron.

[0037] In this embodiment the method of 2) was used to form P-type polycrystalline silicon with an impurity concentration of 1×10^{16} cm^{-3} to 1×10^{21} cm^{-3} by adjusting the diffusion time at 900°C, and the relationship between the impurity concentration of the P-type gate electrode and channel mobility was investigated. To investigate the effect of the silicide film, using a number of samples, refractory metal silicide layers 9 of WSi_2, $MoSi_2$ and $TiSi_2$ were formed on the P-type polycrystalline silicon. The P-type polycrystalline silicon or composite silicide and P-type polycrystalline silicon layer and gate insulation layer were then etched to form the gate electrode. The oxide film over the source and drain regions was then etched to form contact holes. Following this, vapor deposition or sputtering was used to form a metal-containing layer or laminated layer of nickel, titanium or aluminum, and RIE or wet etching was used to form metal wires 10. In this example, vapor deposition of nickel was used, followed by wet etching. To ensure good ohmic contact, the samples were then heat-treated for 5 minutes at 1000°C in an argon atmosphere, thereby completing the fabrication of MIS field-effect transistors.

[0038] Figure 2 shows the measurement-based relationship between channel mobility and threshold voltage in a MIS field-effect transistor with a gate electrode using P-type polycrystalline silicon, N-type polycrystalline silicon, and aluminum. At the same threshold voltage, channel mobility is higher with a gate electrode that uses N-type polycrystalline silicon or aluminum is used, compared to a gate electrode using P-type polycrystalline silicon. This might be attributable to the fact that, depending on the gate electrode polarity, a different amount of ion implantation is required to achieve the same threshold voltage. Implantation of N-type impurity into the buried channel region 2 results in the center of the channel being formed at a deep location, away from the interface between the gate insulation layer and the P-type silicon carbide substrate 1. Since this increases the number of carriers that are not readily susceptible to the effect of the high field near the interface channel mobility is increased. Channel mobility is also increased with increasing concentration of implanted N-type impurity. However, if the N-type impurity in the buried channel region 2 is increased to increase the channel mobility, the threshold voltage tends to decrease, becoming a negative voltage, creating a state in which current flows even at a zero voltage, that is, a normally on state that, in practice, makes it difficult to use the device. It is known that, in general, the larger the difference of work function between gate electrode and semiconductor, the higher the threshold voltage of the MIS field-effect transistor becomes. With reference to the difference of work function between gate electrode and semiconductor, it is also known that there is almost no change when aluminum is used for the gate electrode and the semiconductor is N-type polycrystalline silicon, but with P-type polycrystalline silicon, the difference becomes approximately one volt more. Therefore, even when N-type impurity is implanted in the channel region, the tendency for the threshold voltage to go negative and create a normally on state can be suppressed by using P-type polycrystalline silicon. Thus, even with the same threshold voltage, a higher impurity concentration is implanted in the buried channel region 2 to enable channel mobility to be increased.

[0039] Figure 3 is a measured result showing the L_{bc}/X_j dependency of the channel mobility, when the junction depth X_j of the source/drain diffusion layer is 0.5 μm. In Figure 3, the vertical axis shows the normalized channel mobility of a sample having no buried channel region. The evaluation was performed using an L_{bc}/X_j of 0.2 or above; it was confirmed that there was an effect even at 0.2. Therefore, the lower limit on the horizontal axis was set at 0.2. At over 1 on the horizontal axis, channel mobility increases, but the

threshold voltage goes negative, resulting in a normally on state that makes the device difficult to use. Therefore, the horizontal axis is limited to 0.2 to 1.0. A range of 0.4 to 1.0 is particularly effective.

[0040] Figure 4 shows the measured relationship between the impurity concentration of the P-type polycrystalline silicon gate and the threshold voltage. A higher concentration increases the difference of work function between gate and semiconductor, increasing the threshold voltage. Conversely, a lower concentration decreases the threshold voltage, which at 1 x 10^{16} cm^{-3} becomes zero. Therefore the lower limit for the impurity concentration is set at 1 x 10^{16} cm^{-3} and the upper limit is set at 1 x 10^{21} cm^{-3}.

[0041] Figure 5 shows the measured relationship between channel mobility (using the value at an impurity concentration of zero as the standard value) and the impurity concentration of the buried channel region 2. The lower limit of the evaluation impurity concentration was 5 x 10^{15} cm^{-3}. Since an adequate effect was achieved with that value, the lower limit was set at 5 x 10^{16} cm^{-3}. With a concentration of 1 x 10^{18} cm^{-3} or over, the threshold voltage goes negative, making the device hard to use, so the upper limit was set at 1 x 10^{18} cm^{-3}.

[0042] If the impurity concentration of the P^+ punch-through prevention region provided under the buried channel region 2 to suppress punch-through is lower than 1 x 10^{17} cm^{-3}, the gate voltage that gives rise to punch-through is the same as when there is no P^+ region, meaning there is no effect. A concentration of at least 1 x 10^{17} cm^{-3} increases the gate voltage at which punch-through occurs, so the lower limit was set at 1 x 10^{17} cm^{-3}. When the impurity concentration is 1 x 10^{19} cm^{-3} or higher, the impurity diffuses during activation annealing, offsetting the N-type impurity in the channel region above, making it impossible for the buried channel region to function as required. Therefore, the upper limit was set at 1 x 10^{19} cm^{-3}.

[0043] The resistivity of polycrystalline silicon given a high boron concentration is in the order of several mΩcm, but the resistivity of the refractory metal silicides $MOSi_2$, WSi_2 and $TiSi_2$ are 60 Ωcm, 50 Ωcm and 15 Ωcm, respectively. So, the resistivity of a gate electrode that is a composite of polycrystalline silicon and silicide is lower compared to polycrystalline silicon in which impurity has been implanted. This makes it possible to reduce the resistance of wiring, using long, thin gate electrodes or the gate electrode

formation layer. By using the wiring resistance to reduce the time constant, the operating speed of the device can be improved.

Example 2

[0044] A P-type silicon carbide substrate 1 (impurity concentration: 5×10^{15} cm^{-3}) shown in Figure 1(a) was used. After the substrate 1 was subjected to RCA cleaning, reactive ion etching (RIE) was used to form photolithography alignment marks on the substrate. Next, phosphorus ion implantation was used to form a buried channel region 2 at a junction depth L_{bc} of 0.3, using multiple implantations at 40 keV to 250 keV to provide a total dose for a concentration of 7×10^{15} cm^{-2}. Then, as shown in Figure 1(d), to form an ion implantation mask, an LTO layer was formed over the whole surface and photolithography was used to leave the gate electrode portion resist, with hydrofluoric acid being used to etch the LTO layer. To investigate the hot-carrier resistance effect of the impurity concentration between the buried channel region 2 and the source 5 and drain 6, ion implantation of phosphorus at 500°C was used to form a low-impurity-concentration region 11 between the buried channel region 2 and the source 5 and drain 6 having an impurity concentration of 5×10^{16} cm^{-3} to 5×10^{20} cm^{-3} . To form the source region 5 and drain region 6, an LTO layer was formed over the whole surface and photolithography used to form a photoresist to define the source and drain regions, and hydrofluoric acid was used to etch the LTO and expose the ion implantation source and drain regions. The source 5 and drain 6 were then formed using multiple ion implantations at 500°C to form a phosphorus concentration of 5×10^{19} cm^{-3}. This was followed by activation annealing for 30 minutes at 1500°C in an argon atmosphere, and oxidation at 1200°C for 150 minutes, forming the gate insulation layer 7 approximately 50 nm thick shown in Figure 1(c). After annealing for 30 minutes in an argon atmosphere, the samples were cooled in argon to room temperature. The P-type gate electrode was then formed by using the CVD method to form polycrystalline silicon, using spin-coating to form a boron-containing oxide film or. the polycrystalline silicon, followed by 30 minutes of heat treatment at 900°C to diffuse boron from the boron-containing oxide film to the polycrystalline silicon. The P-type polycrystalline silicon and the gate insulation layer were etched to form the gate electrode. Next, LTO was deposited over the whole surface of the oxide layer and the oxide film over the source 5 and drain 6 was etched to form contact holes. The electron-beam evaporation method was then used to form a nickel over-layer and wet

etching was used to form metal wires 10. To form a good ohmic contact, the samples were then heat-treated for 5 minutes at 1000°C in an argon atmosphere, thereby completing the fabrication of MIS field-effect transistors.

[0045] The transistors were subjected to an electrical stress for a set time and the degree by which the threshold voltage changed was measured to evaluate hot carrier endurance. A smaller change in threshold voltage indicated good hot-carrier endurance. The threshold voltage was defined as the gate voltage that square root of drain current intersects the gate voltage axis, where the drain current was measured as a function of the gate voltage which was swept from 0 V to 30 V with a drain voltage of 0.1 V.

[0046] The electrical stress comprised applying 5 volts to the drain and 2.5 volts to the gate, for five minutes. Ion implantation of phosphorus was used to form an impurity concentration of 5×10^{16} cm^{-3} to 5×10^{19} cm^{-3} between the buried channel region 2 and the source/drain regions. A low impurity concentration in this region will result in a smaller field in the vicinity of the drain, making it possible to prevent electrons that pass through the region from entering a high-energy state, thereby improving hot-carrier endurance by decreasing the number of electrons that is injected into the gate insulation layer from the substrate. However, if the impurity concentration of this region is too low, the resistance of the region will become too high, reducing the driving force of the transistor. Therefore, the lower limit is set at 5×10^{16} cm^{-3}. If the concentration is too high, the field in the vicinity of the drain will not be alleviated, making it impossible to attain sufficient hot-carrier endurance. From measurements, it was found that with a concentration of 5×10^{19} cm^{-3} or higher, the change in threshold voltage exceeded 10%, an amount that makes the device unusable. Therefore, the upper limit was set at 5×10^{19} cm^{-3}.

Example 3

[0047] P-type silicon carbide substrates 1 with hexagonal silicon carbide crystalline (0001) and (11-20) surfaces (impurity concentration: 5×10^{15} cm^{-3}) were subjected to RCA cleaning, and reactive ion etching (RIE) was used to form photolithography alignment marks on the substrates. Phosphorus ion implantation was then used to form a buried channel region 2 at a junction depth L_{bc} of 0.3, using multiple implantations at 40 keV to 250 keV to provide a total dose for a concentration of 7×10^{15} cm^{-2}. Next, to form an ion implantation mask 4 for the source and drain regions shown in Figure 1(b), thermal oxidation or chemical vapor

deposition (CVD) was used to forma SiO_2 layer. As shown in Figure l(b), a low-temperature oxide (LTO) layer was used for the implantation mask. The LTO layer was formed by reacting silane and oxygen at 400°C to 800°C to form silicon dioxide, which was deposited on the substrate 1. A photoresist was then used to define the source and drain regions, and hydrofluoric acid was used to etch the LTO to form an opening to the source/drain regions that are to be subjected to the ion implantation. The source 5 and drain 6 of Figure 1(b) were then formed using phosphorus ion implantation steps effected at 500°C to achieve an impurity concentration of 5×10^{19} cm^{-3}. This was followed by activation annealing for 30 minutes at 1500°C in an argon atmosphere. This was followed by oxidation at 1200°C for 150 minutes, forming the approximately 50 nm gate insulation layer 7, as shown in Figure 1(c). After annealing for 30 minutes in an argon atmosphere, the samples were cooled in argon to room temperature. The P-type gate electrode 8 was then formed using the CVD method to form polycrystalline silicon and using spin-coating to form a boron-containing oxide film on the polycrystalline silicon, followed by 30 minutes of heat treatment at 900°C to diffuse boron from the boron-containing oxide film to the polycrystalline silicon. The P-type polycrystalline silicon and the gate insulation layer were then etched to form the gate electrode. The oxide film over the source and drain regions was then etched to form contact holes. The electron-beam evaporation method was then used to form a nickel over-layer and wet etching was used to form metal wires 10. To form a good ohmic contact, the samples were then heat-treated for 5 minutes at 1000°C in an argon atmosphere, thereby completing the fabrication of the MIS field-effect transistors.

[0048] The MIS field-effect transistors thus fabricated on a (0001) surface had a channel mobility of 70 cm^2/Vs, while MIS field-effect transistors fabricated on a (11-20) surface had a channel mobility of 100 cm^2/Vs. Thus, the channel mobility was improved by fabricating NHS field-effect transistors on a (11-20) surface.

[0049] Figure 6 shows an example of a type of MOSFET structure referred to as a lateral resurf or lateral DMOS type structure. Ion implantation can also be used to form a lateral resurf or lateral DMOS type MOSFET with a P-well, as shown in Figure 7. The P-well is formed as follows. The surface of a P-type epitaxially grown SIC substrate layer is subjected to multiple boron ion implantation steps at 30 to 160 keV, using dosages ranging from 1.5 to 36×10^{13} cm^2, which is followed by 30 minutes of annealing at 1600°C, thereby

forming the P-well. The P-well can also be formed using aluminum. The remaining process steps are the same as those described with respect to the preceding examples.

[0050] The above-described transistor structure can also be applied to the DMOS type MOSFET shown in Figure 8, by making the slight modifications described below. The modifications relate to the substrate and well formation, and require the following additional processes. First, a SiC layer is epitaxially grown on an N^+ substrate, over the drain, and another N^+ layer is formed on the first N^+ layer, and the surface thereof is subjected to multiple boron ion implantation steps at 30 to 160 keV, using dosages ranging from 1.5 to 36 x 10^{13} cm^{-1}, which is followed by 30 minutes of annealing at 1600°C, thereby forming the P-well. The P-well can also be formed using aluminum. The remaining process steps are the same as those described with respect to the preceding examples.

[0051] The DMOS type MOSFET shown in Figure 9 also can be obtained by adding a step of implanting boron ions at 200 to 400 keV using dosages ranging from 3.0 to 10 x 10^{13} cm^{-2} to the steps of the DMOS type MOSFET shown in Figure 8.

[0052] While in the foregoing description the material of the semiconductor region is silicon carbide, the invention is not limited thereto, with the same effect being obtained with a substrate having a semiconductor region of diamond, silicon, gallium nitride or other such semiconductor material.

[0053] The invention comprised as described in the foregoing provides the following effects.

[0054] Using a P-type gate electrode makes it possible to use a relatively high N^- concentration without the device assuming a normally on state, thereby making it possible to increase channel mobility. Channel mobility is also improved when optimizing the ratio between the source/drain junction depth L_{bc} and the junction depth of the buried channel region junction. The channel mobility can also be improved by the optimization of the P-type polycrystalline silicon concentration, and the concentration of the buried channel region.

[0055] Device driving power can be raised when reducing the gate resistance by forming a refractory metal silicide layer over the P-type polycrystalline silicon gate electrode. The operating speed of the SiC semiconductor device can be increased using tungsten, molybdenum or titanium silicide layers. Hot-carrier endurance can be improved by the provision, between the buried channel formation region and the source and drain regions, a region having an impurity concentration that is not lower than the maximum impurity

concentration of the impurity diffusion layer region used to form the buried channel region, and not higher than the impurity concentration of the source and drain regions.

[0056] Punch-through endurance is improved by providing the P-type silicon carbide substrate 1 with a concentrated impurity region that is located beneath the buried channel region, and by optimizing the concentration of the region. Channel mobility is also improved by fabricating the device on the (11-20) surface of a hexagons! or rhombohedral or a (110) surface of a cubic system silicon carbide crystal. A high-power transistor can be readily realized by forming the device as a transistor having a lateral resurf or lateral DMOS type MOSFET structure. Also, the device can be readily fabricated as a normally off transistor by using aluminum or an aluminum alloy for the gate electrode.